IN THE CLAIMS:

Please amend claim 21, as shown in the complete list of claims that is presented below.

Claims 1 and 2. (cancelled).

3. (previously presented) A dry etching method for a semiconductor device, comprising:

providing a polysilicon layer formed on a silicon substrate, the polysilicon layer having an N type region, a P type region, and a non-doped region;

simultaneously gate-etching an N type polysilicon gate electrode from the N type region, a P type polysilicon gate electrode from the P type region, and a non-doped polysilicon arrangement from the non-doped region of the polysilicon layer during a two-stage etching process, the non-doped polysilicon arrangement occupying an area that is larger than a total area occupied by the N type polysilicon gate electrode and the P type polysilicon gate electrode,

wherein an end point detection of one of the stages of the etching process is based on the etching of the non-doped polysilicon arrangement.

Claim 4 (cancelled).

5. (previously presented) The dry etching method according to claim 3, wherein the two-stage etching includes a first stage using a mixed gas of HBr and O_2 and a second stage using a mixed gas of HBr, O_2 and He.

Claims 6-10 (cancelled).

11. (previously presented) The dry etching method according to claim 3, wherein the N type polysilicon gate electrode and the P type polysilicon gate electrode are disposed adjacent one another.

Claims 12-13 (cancelled).

14. (previously presented) The dry etching method of claim 3, wherein the non-doped polysilicon body is disposed adjacent to at least one of the N type polysilicon gate electrode and the P type polysilicon gate electrode.

15. (previously presented) A dry etching method for a semiconductor device, comprising:

providing a polysilicon layer formed on a semiconductor substrate, the polysilicon layer having an N type region, a P type region , and a non-doped region, and

simultaneously etching an N type polysilicon gate electrode from the N type region, a P type polysilicon gate electrode from the P type region, and a non-doped polysilicon arrangement from the non-doped region of the polysilicon layer during an etching process, the non-doped polysilicon arrangement occupying an area that is larger than a total area occupied by the N type polysilicon gate electrode and the P type polysilicon gate electrode,

wherein the etching process includes at least one etching stage in which end point detection is based on the etching of the non-doped polysilicon arrangement.

16. (previously presented) The dry etching method according to claim 15, wherein the non-doped polysilicon body is disposed adjacent at least one of the P type polysilicon gate electrode and the N type polysilicon gate electrode.

17. (previously presented) The dry etching method according to claim 15, wherein the P type polysilicon gate electrode is disposed adjacent to the N type polysilicon gate electrode.

18. (previously presented) The dry etching method according to claim 15, wherein the at least one etching stage is conducted using a mixed gas of HBr and O_2.

19. (previously presented) The dry etching method according to claim 15, wherein the at least one etching stage is conducted using a mixed gas of HBr, O_2, and He.

20. (previously presented) The dry etching method according to claim 15, wherein the semiconductor device has a plurality of transistors when fabrication of the semiconductor device is completed, and wherein the non-doped polysilicon arrangement is electrically disconnected from all of the transistors in the semiconductor device.

21. (currently amended) The dry etching method according to claim 3, wherein the semiconductor device has a plurality of transistors when fabrication of the semiconductor device is completed, and wherein the non-doped polysilicon arrangement is electrically disconnected from all of the transistors in the semiconductor device.